Design and Analysis of Power Efficient PTL Half Subtractor Using 120nm Technology

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ABSTRACT : *In the designing of any VLSI System, arithmetic circuits play a vital role, subtractor circuit is one among them. In this paper a Power efficient Half-Subtractor has been designed using the PTL technique. Subtractor circuit using this technique consumes less power in comparison to the CMOS and TG techniques. The proposed Half-Subtractor circuit using the PTL technique consists of 6 NMOS and 4 PMOS. The proposed PTL Half-Subtractor is designed and simulated using DSCH 3.1 and Microwind 3.1 on 120nm. The power estimation and simulation of layout has been done for the proposed PTL half-Subtractor design. Power comparison on BSIM-4 and LEVEL-3 has been performed with respect to the supply voltage on 120nm. Results show that area consumed by the proposed PTL Half-Subtractor is 147.8μm^2 on 120nm technology. At 1V power supply the proposed PTL Half-Subtractor consumes 3.353μW power on BSIM-4 and 3.546μW power on LEVEL-3. The proposed circuit has also been compared with other Subtractor designs using CMOS and TG logics, and the proposed design has been proven power efficient as compared to design by other logics.*

Keywords – *AVLG, AVLS, BSIM, CMOS, DSCH, Gate Diffusion Input, PTL, Transmission Gate*

I. INTRODUCTION

In very large scale integration the increasing demand for low power can be addressed at different logic levels, such as circuit, architectural and layout. At circuit design level considerable amount of power can be saved by means of proper choice of a logic style. The proper choice of a logic style is important because all important parameters governing power dissipation- switching capacitance, transition activity, and short circuit currents- are strongly influenced by the chosen logic style [1]. The increasing eminence of portable systems and the need to limit power consumption in very high density ULSI chips have led to rapid and very interesting developments in low-power design in recent years [2]. A one such combinational circuit that performs the subtraction of two bits is called a half-subtractor. The digit from which another digit is subtracted is called the minuend and the digit which is to be subtracted is called the subtrahend. There are a number of logic styles by which a circuit can be implemented some of them used in this paper are CMOS, TG, PTL. CMOS logic styles are robust against voltage scaling and transistor sizing and thus provide a reliable operation at low voltages and arbitrary transistor sizes. In CMOS style input signals are connected to transistor gates only, which facilitate the usage and characterization of logic cells. Due to the complementary transistor pairs the layout of CMOS gates is not much complicated and is power efficient. The large number of PMOS transistors used in complementary CMOS logic style is one of its major disadvantages and it results in high input loads [3].

The transmission gate is simply the combination of two complementary transistors. These gates are more often used internally in larger scale CMOS devices because of its simplicity and low propagation delay. The advantage of pass transistor logic is that it uses smaller number of transistors and smaller input loads, especially when NMOS transistors are used. Thus in this paper the use of PTL logic has been made for the reduction of power dissipation.

II. SCHEMATIC CIRCUIT

The half subtractor is a combinational circuit that is used to perform the subtraction of two bits. It consists of two inputs called the minuend and the subtrahend and two outputs called difference and borrow. The minuend is denoted by input A, the subtrahend is denoted by input and the two outputs are denoted by D_0 and B_0 respectively. The logic diagram for half subtractor is shown in Fig. 1.

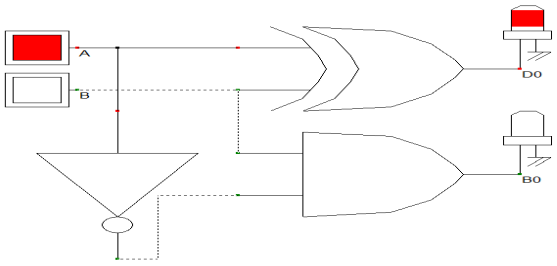


Fig. 1 Half subtractor Logic Diagram [4]

The Boolean expression for the two output variables are as follows

$$D_0 = \overline{A}.B + A.\overline{B}$$

(1) $B_0 = \overline{A}.B$ (2)

The Truth table of Half- Subtractor has been shown in Table 1.

Table.1. Truth Table of Half Subtractor

A	B	D_0	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

III. PREVIOUS WORK

In the literature [5]-[6], the half subtractor is implemented with two different techniques called the AVLG and AVLS techniques. Fig. 2 and 3 shows the half subtractor using AVLG and AVLS technique on 90nm.

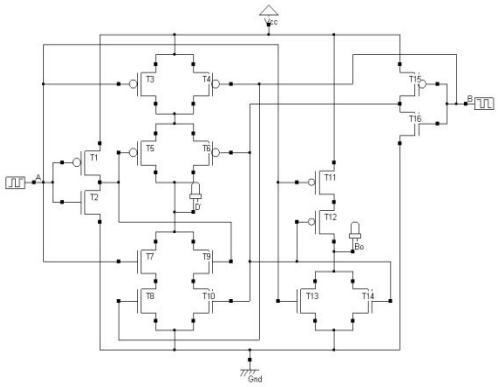


Fig.2. Transistor level Half-Subtractor Circuit [5]

In Fig. 2 a half subtractor circuit using 16 transistors has been shown. If a conventional half subtractor is designed on the MICROWIND software, the power consumed is about 18.539µW [5] which is a very large value and may lead to heating of the system.

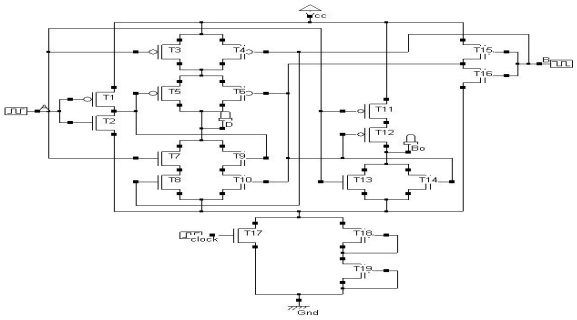


Fig.3. Half-Subtractor using AVLG Technique [5]

In order to reduce the power consumed two techniques namely The AVLS (Adaptive Voltage Level at Supply) technique shown in Fig.4 which the supply voltage is reduced and AVLG (Adaptive Voltage Level at Ground) in which the ground potential is increased are used. This subtractor circuit consists of 8T PMOS and 8T NMOS transistors. In AVLG Technique the adaptive voltage level control circuit is used at the lower end of the cell to lift the potential of the ground node. The use of AVLG Technique decreases the power consumption through an added gate T17. T17 gate is N-MOS in nature. Therefore, this approach is useful in lowering the final value of the power consumption. This technique makes use of 19 transistors and consumes 233µW power.

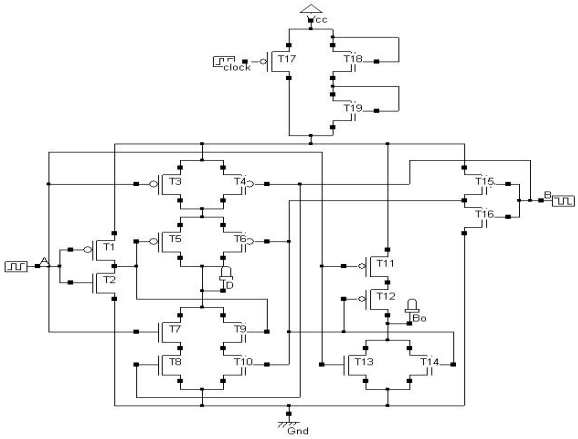


Fig.4. Half Subtractor using AVLS Technique [5]

In AVLS Technique the adaptive voltage level control circuit is used either at the upper end of the cell to bring down the supply voltage value. In this technique a decrease in power consumption of the circuit is brought due to the reduction in drain voltages in transistors T2, T3, T6. In comparison to the AVLG approach this approach is more successful in lowering the value of the

total power usage. This technique also consists of 19 transistors and produces a power of 67.182µW.

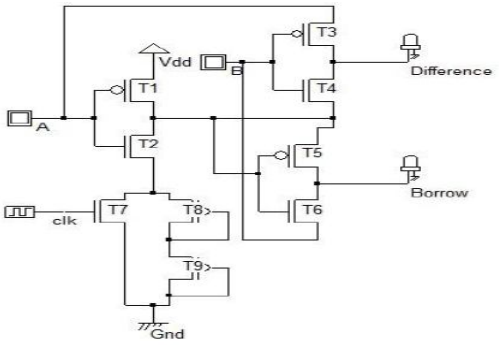


Fig.5. Half Subtractor using AVLG [6]

Fig. 5 shows the logic circuit of half subtractor circuit using AVLG technique on 65nm. In this technique, 1 NMOS and 2 PMOS combination is connected in parallel. An input clock pulse is applied to the N-MOS of circuit and rest all P-MOS are connected to ground. This half subtractor using AVLG technique on 65nm makes use of 9 transistors and consumes 2.321µW power.

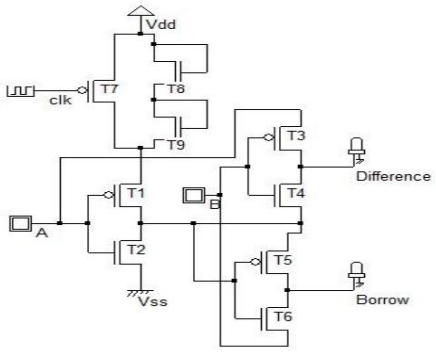


Fig.6. Half Subtractor using AVLS technique [6].

Fig. 6 shows the logic circuit of half subtractor circuit using AVLS technique on 65nm. In this technique, 2 NMOS and 1 PMOS combination is connected in parallel. An input clock pulse is applied at the P-MOS of circuit and rest all N-MOS are connected to drain terminal. This technique also uses 9 transistors and consumes 1.622µW power.

IV. XOR MODULE

In the recent past various approaches of CMOS design by using various area and power efficient logic styles has presented by the researchers in literature. Area consumption by the design, delay introduced by the circuit and power consumed by the circuit are the main criteria of concern in CMOS circuit design which often conflict with the design methodology and act as a constrain on the design of any CMOS circuits. These performance criteria's i.e. area, power and delay should be individually investigated, analyzed and their interaction to develop both quantitative and qualitative understanding of the various designs has been presented in literature.

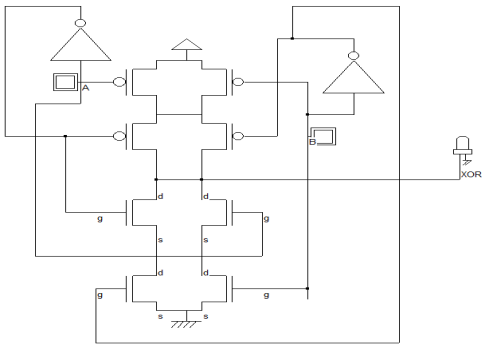


Fig.7. CMOS XOR Design

Different XOR designs by using different logic styles have been presented in literature. In [7-8] CMOS and TG Full adder Designs by using CMOS and TG XOR designs have been presented. These XOR designs by using CMOS and TG logic have been shown in Fig.7 and Fig.8. A CMOS and TG XOR design provides full voltage swing between 0 and VDD. But disadvantage of these designs is that they consume large power and area as compare to PTL and GDI. Also other designs by using pseudo NMOS logic style and by using pass transistor logic have been presented which consumes less area as compare to the CMOS and TG designs but at the output there can be threshold loss problem. But CMOS and TG show full voltage swing at the output as compare to the Pass transistor based XOR design.

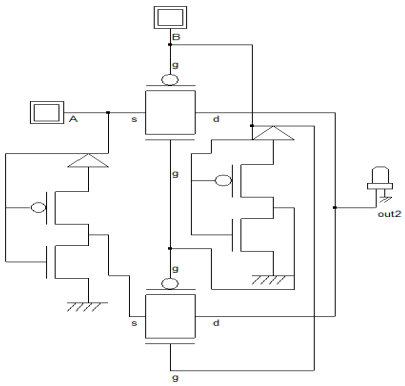


Fig.8. TG XOR Design

XOR is a basic building block of half Subtractor architecture. So if the transistor count in XOR circuit can be reduced it can further decrease the area consumption of half Subtractor. A 4T XOR design has been shown in Fig.9 [8]. Disadvantage of this circuit is threshold loss problem which can be overcome by inverted buffered XOR/XNOR design. Although threshold loss problem is common in PTL design but it has advantage of less area.

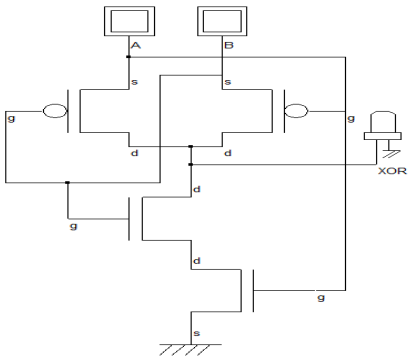


Fig.9. PTL XOR Design

Also in this paper [8] PTL and inverter based XOR/XNOR circuits and 4 different 2x1 MUX are also shown by the authors. This XOR design has highest working frequency, low power and area consumption compared to CMOS and TG designs. GDI approach is very efficient for high speed, low power circuits with improved logic level swing and static power characteristics using a reduced number of transistors as compared to CMOS and TG techniques.

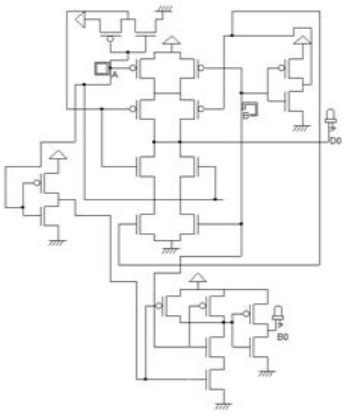


Fig.10.a CMOS Half- Subtractor Design

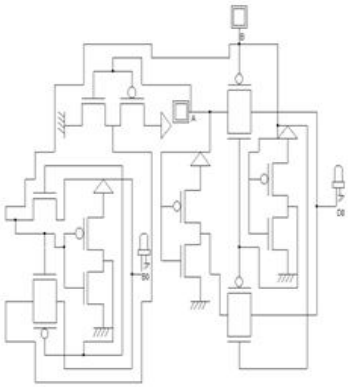


Fig.10.b TG Half-Subtractor Design

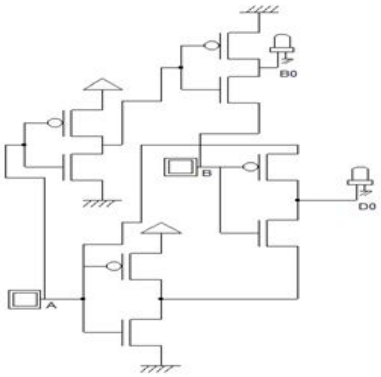


Fig.10.c GDI Half-Subtractor Design

Fig.10. Half-Subtractor Design

In [9] XOR function is achieved by using GDI technique shown in Fig.11. XOR circuit by using this technique uses 4 transistors to generate balanced XOR output. Same GDI cell is used with different Logic functions to get XOR output which is difference output of the half Subtractor.

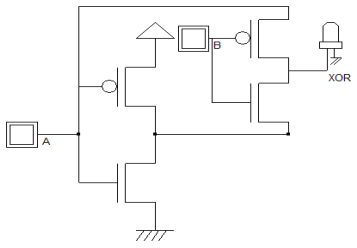


Fig.11. GDI XOR design

V. PROPOSED HALF-SUBTRACTOR DESIGN

The proposed PTL Half Subtractor has been shown in Fig.12. It consists of The XOR module and it is designed by the PTL Logic which is power efficient in comparison to the TG, CMOS and GDI. The other modules used here are the AND gate and the inverter gate. The AND gate using PTL logic consists of 4 transistors. The proposed PTL half Subtractor is implemented by using 10 transistors and is power efficient in comparison to the other logics. The difference output has been obtained directly from the XOR module, while the borrow output has been obtained by the combination of all three gates i.e. AND, XOR and the INVERTER. The timing simulation of half subtractor has been obtained on DSCH 3.1 and then post layout simulation has been seen on MICROWIND 3.1.

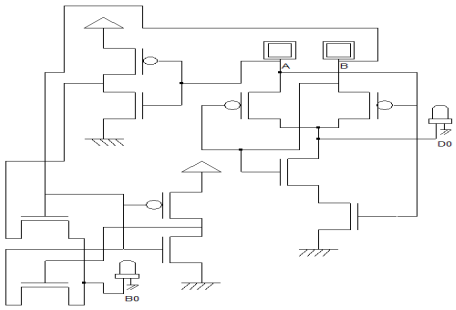


Fig.12. Proposed PTL Half-Subtractor Design

VI. LAYOUT ANALYSIS

Manual layout is very difficult for those design which consists large no of gates for its construction. In complex VLSI design manual layout designing for a very complex circuit will become very difficult. So an automatic layout generation approach is preferred as compared to manual layout designing. Post layout simulation and Layout diagram of half subtractor has been shown in Fig.14 and 15 respectively

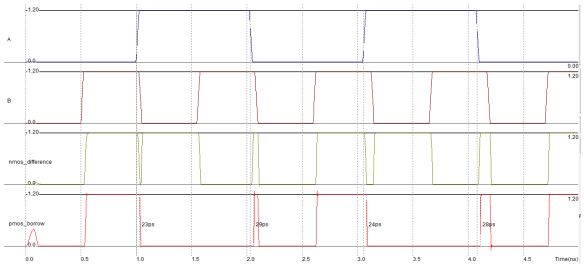


Fig.14 Post Layout Simulation of PTL Half Subtractor

Fig.13 shows the timing simulation of proposed half subtractor design. Simulation has been done on DSCH designing tool to get the timing waveform. From the Fig.13 it is seen that the timing waveform is generated for the two outputs according to the truth table. Timing simulation shows the exact functionality of half subtractor for two outputs. Proposed PTL half subtractor has been validated in terms of power on MICROWIND 3.1.

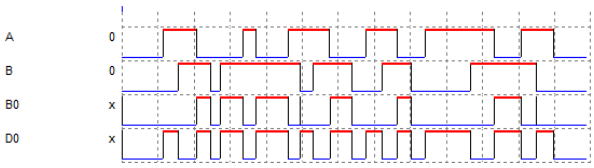


Fig.13 Timing Simulation of GDI 1- Bit Subtractor

Different Half Subtractor designs have been shown in Fig. 10 by using conventional CMOS, TG and GDI logics. Half Subtractor design by conventional CMOS consist 20 transistors, TG Subtractor consist 15 transistors and GDI Subtractor consist 8 transistors respectively in half subtractor designs.

In DSCH designing tool the schematic diagram has been firstly designed and validated at logic level on DSCH designing tool. Although DSCH 3.1 have feature to analyze timing simulation as well as power consumption at logic level but accurate layout information is still missing.

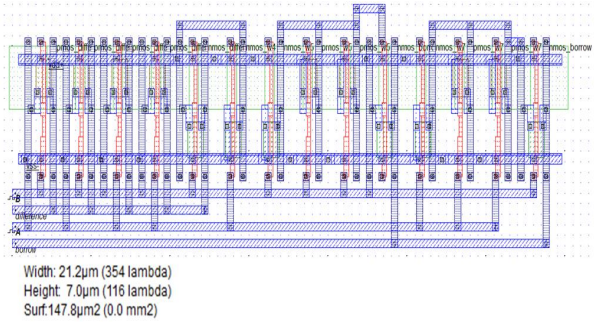


Fig.15 Layout of PTL Half Subtractor

VERILOG file is generated by the DSCH 3.1 tool which is compiled by the MICROWIND to construct the corresponding layout with exact desired design rules. Another way to create the design is by NMOS and

PMOS devices using cell generator provided by the MICROWIND 3.1. The advantage of this approach is to avoid any design rule error. Length and width can be adjusted by the MOS generator option on MICROWIND tool.

VII. POST LAYOUT SIMULATION

The evaluation of proposed PTL Half-Subtractor design has been done in terms of power on 120nm technology. MICROWIND 3.1 has been used for simulation in terms of variation in power with respect to the variation in voltage on LEVEL-3 and BSIM-4 and the results are measured on both BSIM-4 and LEVEL-3.

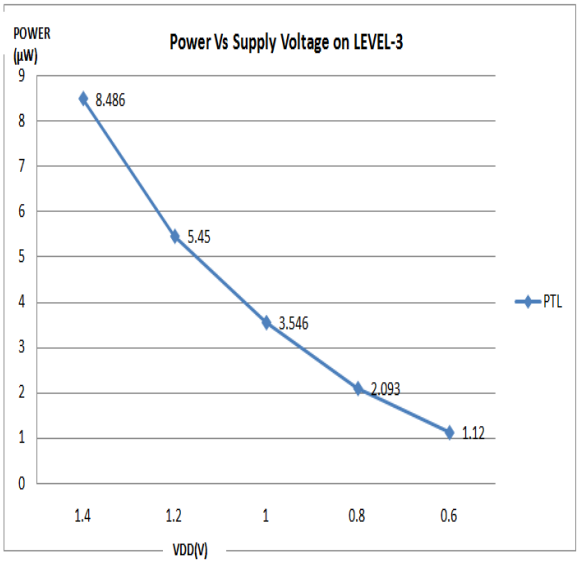


Fig.16. Power Vs Supply Voltage on Level 3

MOS Empherical model Level-3 and BSIM Model-4 at different power Vdd are used for performing the simulation. 0.4 V has been taken as the threshold voltage for both the levels. MOS Empherical model Level-3 and BSIM Model-4 has been used to measure power variation on voltage levels 0.6, 0.8, 1, 1.2 and 1.4V.

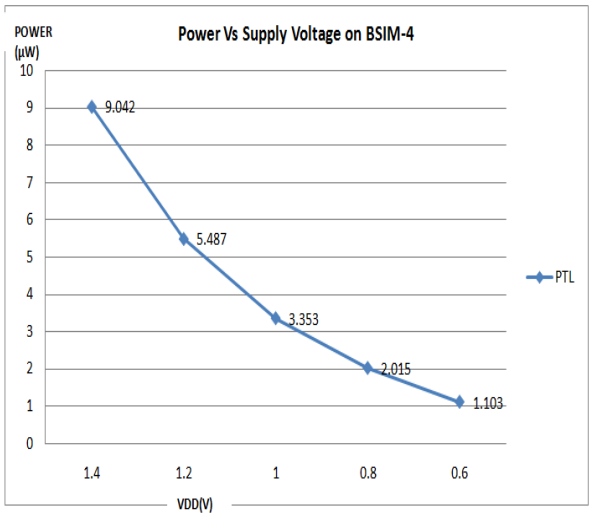
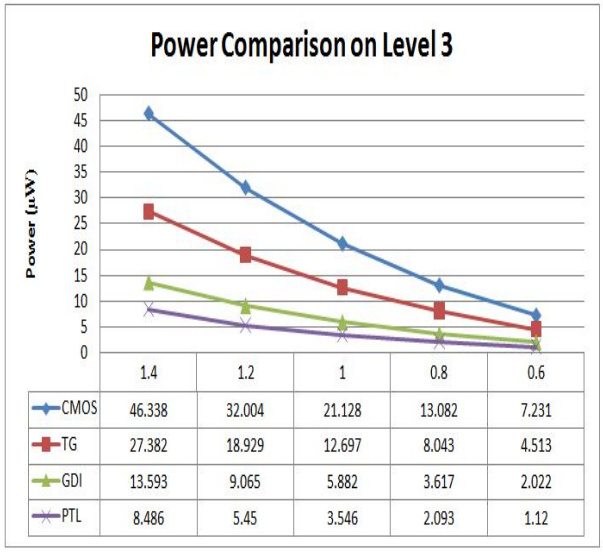


Fig.17. Power Vs Supply Voltage on BSIM-4

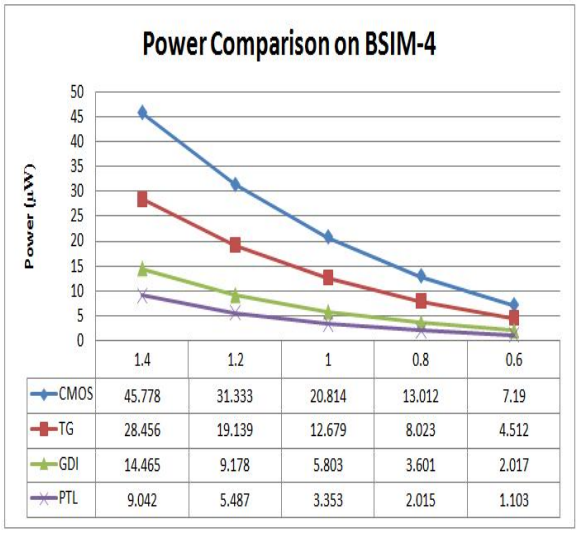
10 different curve fitting parameters have been used in MOS Empherical model Level-3 whereas BSIM Model-4 works with 19 different parameters. Results for change in power w.r.t voltage are plotted for proposed half subtractor design and shown in Fig.16 for LEVEL-3 and in Fig. 17 for BSIM-4. With respect to VDD the results show non-linear dependence of power on supply voltage. For different technologies such as 120mm, 90mm etc layout result will change for same circuit. Analog simulation is carried out on Microwind 3.1for proposed PTL Half- Subtractor on 120nm technology.



	1.4	1.2	1	0.8	0.6
CMOS	46.338	32.004	21.128	13.082	7.231
TG	27.382	18.929	12.697	8.043	4.513
GDI	13.593	9.065	5.882	3.617	2.022
PTL	8.486	5.45	3.546	2.093	1.12

Fig.18 Power Consumption Comparison on BSIM-4

Comparison results for Simulation have been shown in Fig.18 and 19. From Fig.18 and 19 it is clear that power dissipation decreases with decrease in power supply. Fig. 18 and 19 also shows that the power dissipation in BSIM-4 at 1V is less in comparison to LEVEL-3 at 1.2V input supply.



	1.4	1.2	1	0.8	0.6
CMOS	45.778	31.333	20.814	13.012	7.19
TG	28.456	19.139	12.679	8.023	4.512
GDI	14.465	9.178	5.803	3.601	2.017
PTL	9.042	5.487	3.353	2.015	1.103

Fig.19. Power Consumption Comparison on BSIM-4

From the Fig. 19 it is observed that PTL shows improvement of 83%, 73% and 42% as compared to CMOS, TG and GDI techniques respectively on BSIM-4 simulation model.

VIII. CONCLUSION

A half- subtractor using PTL approaches been designed. The designed half- Subtractor has been implemented using 4 PMOS and 6 NMOS transistors i.e. it consists of total of 10 transistors. The half- subtractor designed by using the PTL approach is a power efficient design as compared to other designs by CMOS, TG and GDI logic. All power results have been simulated on Microwind 3.1. The simulated results are shown on LEVEL-3 and BSIM-4 models using the 120nm technology. The major module used in the proposed design is the XOR module. The proposed PTL Half-Subtractor consumes 3.353µW power on BSIM and 3.546 µW power on Level-3 model on 1V supply voltage. The limitation of PTL half Subtractor is that its surface area is more in comparison to the GDI approach. The GDI approach has a surface area of 136.6µm^2 whereas the PTL approach has the surface area 147.8 µm^2. Thus the future scope of this research could be extended to reducing the surface area, and working parameters like speed, delay, current etc on different neno technology.

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